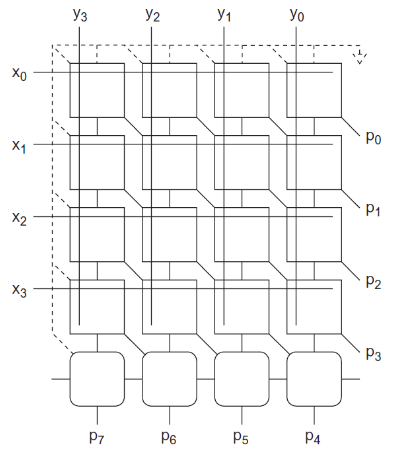
ETICD: Final Project

4x4 bit multiplier

Group 3

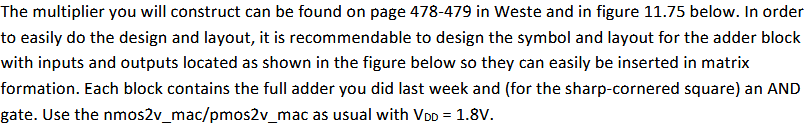
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Figur 1: 4x4 bit multiplier design

# The task:



# Creating the Full adder schematic:

The full 4x4 bit multiplier is made out of several full adders but together in a 4 by 4 array like figure 1, so we started by making a single full adder in Cadence .

Due to the size of the schematic, putting this full adder into a grid would require a lot of extra work, so we instead made a symbol in Cadence representing the full adder:

## Analysing the Full adder:

After creating the symbol we made, a simple testbench to test, whether the logic table of our full adder matches the theoretic one, with a simple DC simulation.

# Creating the full 4x4 bit multiplier schematic:

After testing the Full adder we created a new schematic, where we set up the full 4x4 bit multiplier with our

## Analyzing the 4x4 bit schematic:

First we used a square pulse signal, to check the on and off delay.

Then we need to find the power consumption

# Creating the layout for the full adder:

## Doing the post-layout simulations for full adder:

The D-something simulation

The V-something simulation